IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Kuen-Chyr Lee, et al.	§	Docket No.:	2001-1693 / 24061.450
Serial No.: 10/785,524	§	Customer No.	42717
Filed: February 24, 2004	§	Group Art Unit:	2823
For: Method for Improving the Electrical Continuity for a Silicon-Germanium Film Across a Silicon/Oxide/Polysilicon Surface Using a Novel Two-Temperature Process	§	Examiner:	Trung Q. Dang

DECLARATION UNDER 37 C.F.R. § 1.131

I, Kuen-Chyr Lee, declare and say that:

1. I am a joint inventor of the subject matter disclosed and claimed in the above-identified application.

2. At all times set forth herein, I was employed at Taiwan Semiconductor Manufacturing Co., LTD, ("TSMC") Hsin-Chu, Taiwan. TSMC is the assignee of the above-identified application.

3. Prior to March 31, 2003, we reduced the subject matter of the present invention to practice, prepared a TSMC Invention Disclosure, and submitted it to TSMC for processing for a patent application. A copy of the original TSMC Invention Disclosure, with dates redacted, is attached as Exhibit A.

4. The TSMC Invention Disclosure of Exhibit A includes two photomicrographs, Figure 3 and Figure 4, of an HBT device that we successfully reduced to practice prior to March 31, 2003, using a two-temperature semiconductor process described in the above-identified application, wherein a blanket seed layer was deposited on a substrate and a patterned polysilicon layer at a first temperature, and then an in-situ doped silicon-germanium layer was formed on the silicon cap layer at a lower temperature.

5. All of the activities described above occurred in Taiwan.

I declare that all statements made herein of my knowledge are true and that all statements made on information and belief are believed to be true and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Kuen-Chyr Lee

Kuen-Chyr Lee

Date: 5, 19, 2005

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Kuen-Chyr Lee, et al.	§	Docket No.:	2001-1693 / 24061.450
	§		
	§	Customer No.	42717
Serial No.: 10/785,524	§		
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Filed: February 24, 2004	§		
	§	Examiner:	Trung Q. Dang
For: Method for Improving the Electrical Continuity for a Silicon-Germanium Film Across a Silicon/Oxide/Polysilicon Surface Using a Novel Two-Temperature Process	§		

DECLARATION UNDER 37 C.F.R. § 1.131

I, Liang-Gi Yao, declare and say that:

1. I am a joint inventor of the subject matter disclosed and claimed in the above-identified application.

2. At all times set forth herein, I was employed at Taiwan Semiconductor Manufacturing Co., LTD, ("TSMC") Hsin-Chu, Taiwan. TSMC is the assignee of the above-identified application.

3. Prior to March 31, 2003, we reduced the subject matter of the present invention to practice, prepared a TSMC Invention Disclosure, and submitted it to TSMC for processing for a patent application. A copy of the original TSMC Invention Disclosure, with dates redacted, is attached as Exhibit A.

4. The TSMC Invention Disclosure of Exhibit A includes two photomicrographs, Figure 3 and Figure 4, of an HBT device that we successfully reduced to practice prior to March 31, 2003, using a two-temperature semiconductor process described in the above-identified application, wherein a blanket seed layer was deposited on a substrate and a patterned polysilicon layer at a first temperature, and then an in-situ doped silicon-germanium layer was formed on the silicon cap layer at a lower temperature.

5. All of the activities described above occurred in Taiwan.

I declare that all statements made herein of my knowledge are true and that all statements made on information and belief are believed to be true and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Liang-Gi Yao

Liang-Gi Yao

Date: May 9, 2005

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Kuen-Chyr Lee, et al.	§	Docket No.:	2001-1693 / 24061.450
Serial No.: 10/785,524	§	Customer No.	42717
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DECLARATION UNDER 37 C.F.R. § 1.131

I, Tien-Chih Chang, declare and say that:

1. I am a joint inventor of the subject matter disclosed and claimed in the above-identified application.

2. At all times set forth herein, I was employed at Taiwan Semiconductor Manufacturing Co., LTD, ("TSMC") Hsin-Chu, Taiwan. TSMC is the assignee of the above-identified application.

3. Prior to March 31, 2003, we reduced the subject matter of the present invention to practice, prepared a TSMC Invention Disclosure, and submitted it to TSMC for processing for a patent application. A copy of the original TSMC Invention Disclosure, with dates redacted, is attached as Exhibit A.

4. The TSMC Invention Disclosure of Exhibit A includes two photomicrographs, Figure 3 and Figure 4, of an HBT device that we successfully reduced to practice prior to March 31, 2003, using a two-temperature semiconductor process described in the above-identified application, wherein a blanket seed layer was deposited on a substrate and a patterned polysilicon layer at a first temperature, and then an in-situ doped silicon-germanium layer was formed on the silicon cap layer at a lower temperature.

5. All of the activities described above occurred in Taiwan.

I declare that all statements made herein of my knowledge are true and that all statements made on information and belief are believed to be true and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Tien-Chih Chang

Tien-Chih Chang

Date: 2005/05/23

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Kuen-Chyr Lee, et al.	§	Docket No.:	2001-1693 / 24061.450
Serial No.: 10/785,524	§	Customer No.	42717
Filed: February 24, 2004	§	Group Art Unit:	2823
For: Method for Improving the Electrical Continuity for a Silicon-Germanium Film Across a Silicon/Oxide/Polysilicon Surface Using a Novel Two-Temperature Process	§	Examiner:	Trung Q. Dang

DECLARATION UNDER 37 C.F.R. § 1.131

I, Chia-Lin Chen, declare and say that:

1. I am a joint inventor of the subject matter disclosed and claimed in the above-identified application.

2. At all times set forth herein, I was employed at Taiwan Semiconductor Manufacturing Co., LTD, ("TSMC") Hsin-Chu, Taiwan. TSMC is the assignee of the above-identified application.

3. Prior to March 31, 2003, we reduced the subject matter of the present invention to practice, prepared a TSMC Invention Disclosure, and submitted it to TSMC for processing for a patent application. A copy of the original TSMC Invention Disclosure, with dates redacted, is attached as Exhibit A.

4. The TSMC Invention Disclosure of Exhibit A includes two photomicrographs, Figure 3 and Figure 4, of an HBT device that we successfully reduced to practice prior to March 31, 2003, using a two-temperature semiconductor process described in the above-identified application, wherein a blanket seed layer was deposited on a substrate and a patterned polysilicon layer at a first temperature, and then an in-situ doped silicon-germanium layer was formed on the silicon cap layer at a lower temperature.

5. All of the activities described above occurred in Taiwan.

I declare that all statements made herein of my knowledge are true and that all statements made on information and belief are believed to be true and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Chia-Lin Chen

Chia-Lin Chen

Date: 05/09/2005

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Kuen-Chyr Lee, et al.	§	Docket No.:	2001-1693 / 24061.450
Serial No.: 10/785,524	§	Customer No.	42717
Filed: February 24, 2004	§	Group Art Unit:	2823
For: Method for Improving the Electrical Continuity for a Silicon-Germanium Film Across a Silicon/Oxide/Polysilicon Surface Using a Novel Two-Temperature Process	§	Examiner:	Trung Q. Dang

DECLARATION UNDER 37 C.F.R. § 1.131

I, Shih-Chang Chen, declare and say that:

1. I am a joint inventor of the subject matter disclosed and claimed in the above-identified application.

2. At all times set forth herein, I was employed at Taiwan Semiconductor Manufacturing Co., LTD, ("TSMC") Hsin-Chu, Taiwan. TSMC is the assignee of the above-identified application.

3. Prior to March 31, 2003, we reduced the subject matter of the present invention to practice, prepared a TSMC Invention Disclosure, and submitted it to TSMC for processing for a patent application. A copy of the original TSMC Invention Disclosure, with dates redacted, is attached as Exhibit A.

4. The TSMC Invention Disclosure of Exhibit A includes two photomicrographs, Figure 3 and Figure 4, of an HBT device that we successfully reduced to practice prior to March 31, 2003, using a two-temperature semiconductor process described in the above-identified application, wherein a blanket seed layer was deposited on a substrate and a patterned polysilicon layer at a first temperature, and then an in-situ doped silicon-germanium layer was formed on the silicon cap layer at a lower temperature.

5. All of the activities described above occurred in Taiwan.

I declare that all statements made herein of my knowledge are true and that all statements made on information and belief are believed to be true and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Shih-Chang Chen

Shih-Chang Chen

Date: 050506

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Kuen-Chyr Lee, et al.	Docket No.:	2001-1693 / 24061.450
Serial No.:	10/785,524	Customer No.	42717
Filed:	February 24, 2004	Group Art Unit:	2823
For:	Method for Improving the Electrical Continuity for a Silicon-Germanium Film Across a Silicon/Oxide/Polysilicon Surface Using a Novel Two-Temperature Process	Examiner:	Trung Q. Dang

DECLARATION UNDER 37 C.F.R. § 1.131

I, Mong-Song Liang, declare and say that:

1. I am a joint inventor of the subject matter disclosed and claimed in the above-identified application.

2. At all times set forth herein, I was employed at Taiwan Semiconductor Manufacturing Co., LTD, ("TSMC") Hsin-Chu, Taiwan. TSMC is the assignee of the above-identified application.

3. Prior to March 31, 2003, we reduced the subject matter of the present invention to practice, prepared a TSMC Invention Disclosure, and submitted it to TSMC for processing for a patent application. A copy of the original TSMC Invention Disclosure, with dates redacted, is attached as Exhibit A.

4. The TSMC Invention Disclosure of Exhibit A includes two photomicrographs, Figure 3 and Figure 4, of an HBT device that we successfully reduced to practice prior to March 31, 2003, using a two-temperature semiconductor process described in the above-identified application, wherein a blanket seed layer was deposited on a substrate and a patterned polysilicon layer at a first temperature, and then an in-situ doped silicon-germanium layer was formed on the silicon cap layer at a lower temperature.

5. All of the activities described above occurred in Taiwan.

I declare that all statements made herein of my knowledge are true and that all statements made on information and belief are believed to be true and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Mong-Song Liang

Date: May 6 '08

EXHIBIT A

tsmc 台灣積體電路 TSMC INVENTION DISCLOSURE

EMP. NO.	FULL NAME(S) OF INVENTOR(S)		DEPT.	DEPT. CODE	TEL. NO.	E-Mail	SECURITY B TSMC-RESTRICTED
	ENGLISH	CHINESE					FOR USE BY PATENT AFFAIRS DEPARTMENT
014955	Kuen-Chyr Lee	李崑池	TFD	2331	7034042	KCLEEC@TSMC.COM.TW	DISCLOSURE NO.: 2001-1693 TSMC0
014959	Liang-Gi Yao	姚亮吉	TFD	2331	7034736	LGYAO@TSMC.COM.TW	
014956	Tien-Chih Chang	張添智	TFD	2331	7031214	TCCHANGF@TSMC.COM.TW	RECEIVED DATE: (TIME STAMP)
020388	Chia-Lin Chen	陳佳麟	TFD	2331	7031214	CLCHENV@tsmc.com.tw	
015251	Shih-Chang Chen	陳世昌	TFD	2331	7034746	SCCHENL@TSMC.COM.TW	
002872	Mong-Song Liang	梁孟松	AMTD	2330	7034789	MSLIANG@tsmc.com.tw	柳曼涛 Mandy Liu 707-2385

- TITLE OF INVENTION --

ENGLISH --**DISCONTINUITY IMPROVEMENT FOR SIGE DEPOSITION BETWEEN SI/OXIDE/POLY FILM BY TEMPERATURE ADJUSTMENT WITHOUT SIGE/B PROFILE CHANGE**

- BACKGROUND INFORMATION – CURRENT PRACTICE AND DISADVANTAGES

The SiGe heterojunction bipolar transistor(HBT) has attracted much attention because of both the device performance and the low cost for many applications. The discontinuity phenomenon present during SiGe deposition between Si/oxide/poly film will cause the poor poly sheet resistance connected with base electrode. This patent presents a methodology for discontinuity improvement during SiGe deposition between Si/oxide/poly film by temperature adjustment without changing SiGe/B profile.

- MAIN POINTS OF CLAIM (PLEASE LIST ITEM BY ITEM; 利用何種方法/手段達到目的)

In order to improve discontinuity during SiGe deposition between Si/oxide/poly film by temperature adjustment without changing SiGe/B profile, we only adjust the process temperature of seed layer, and keep the temperature of SiGe and cap deposition the same as standard recipe. That could gain two following advantages:

1.The discontinuity of seed layer was improved by process temperature adjustment.

2.The SiGe/B profile will not be changed because the process temperature of SiGe and cap deposition keep the same.

- PROBLEM SOLVED OR IMPROVEMENTS OBTAINED BY THIS INVENTION (PLEASE LIST ITEM BY ITEM)

Discontinuity present during SiGe deposition between Si/oxide/poly film by temperature adjustment is improved but without changing SiGe/B profile

- KEYWORD SEARCH FOR PATENT/LITERATURES

Discontinuity, temperature, SiGe

- PATENT/ LITERATURES SEARCH RESULT (PLEASE SPECIFY SIMILAR PATENT NO. AND

LITERATURE CITATION)

None

- DETAIL DESCRIPTION OF INVENTION

The discontinuity phenomenon present during SiGe deposition between Si/oxide/poly film will cause the poor poly sheet resistance connected with base electrode. Figure 1 and Figure 2(See attached) shows the discontinuity phenomenon with top view and cross section view during SiGe deposition between Si/oxide/poly film. This patent presents the mothodology that only adjust the process temperature of seed layer, and keep the temperature of SiGe and cap deposition the same with standard recipe.

The results were shown in Figure 3 and Figure 4 (See attached) . That could gain two following advantages:

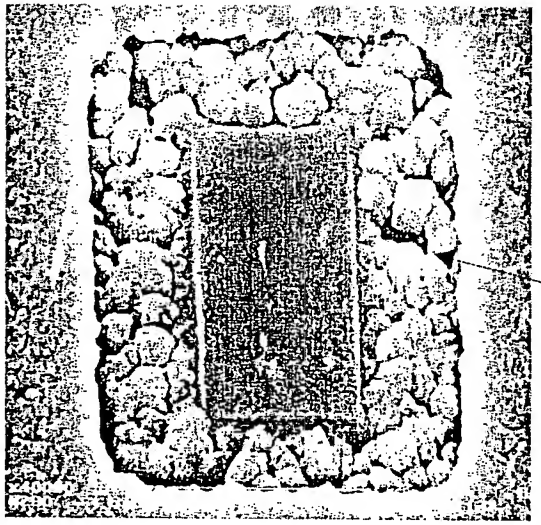
1.The discontinuity of seed layer was improved by process temperature adjustment.

2.The SiGe/B profile will not be changed due to the process temperature of SiGe and cap deposition keep the same.

ATTACHMENTS: 121201.ppt

WITNESS: THE TWO WITNESSES WHOSE SIGNATURES APPEAR BELOW HAVE READ AND UNDERSTOOD THIS ENTIRE INVENTION DISCLOSURE.	SIGNATURE OF WITNESS	DATE	SIGNATURE OF WITNESS	DATE
	黃仁宏		許財傳	

DISCLOSURE SUBMITTED BY			
INVENTORS' EMPNO	INVENTORS' NAME	INVENTOR'S SIGNATURE	DATE
014955	李崑池	李崑池	
014959	姚亮吉	姚亮吉	
014956	張添智	張添智	
020388	陳佳麟	陳佳麟	
015251	陳世昌	陳世昌	
002872	梁孟松	梁孟松	



discontinuity

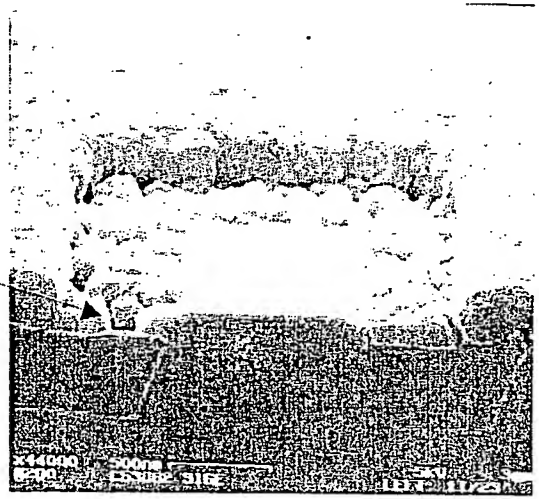
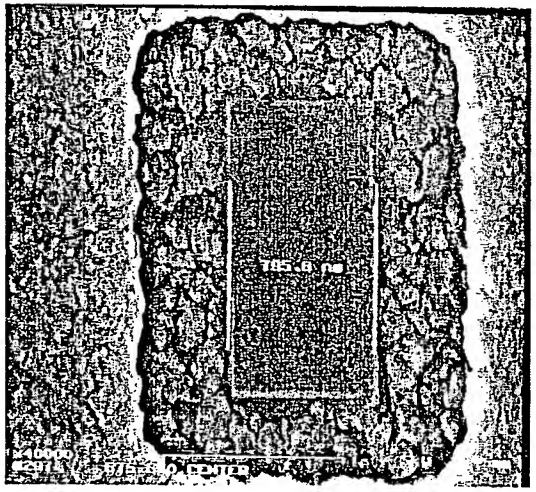


Figure 1

Figure 2



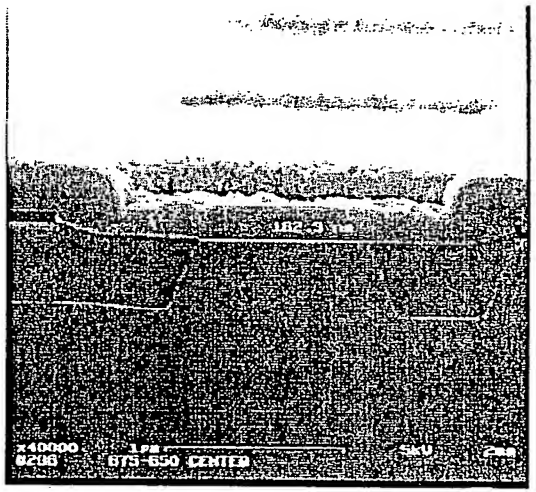


Figure 3

Figure 4

Discontinuity Prevention during SiGe deposition between Si/Oxide/Poly film by Temperature Adjustment without SiGe/B profile change

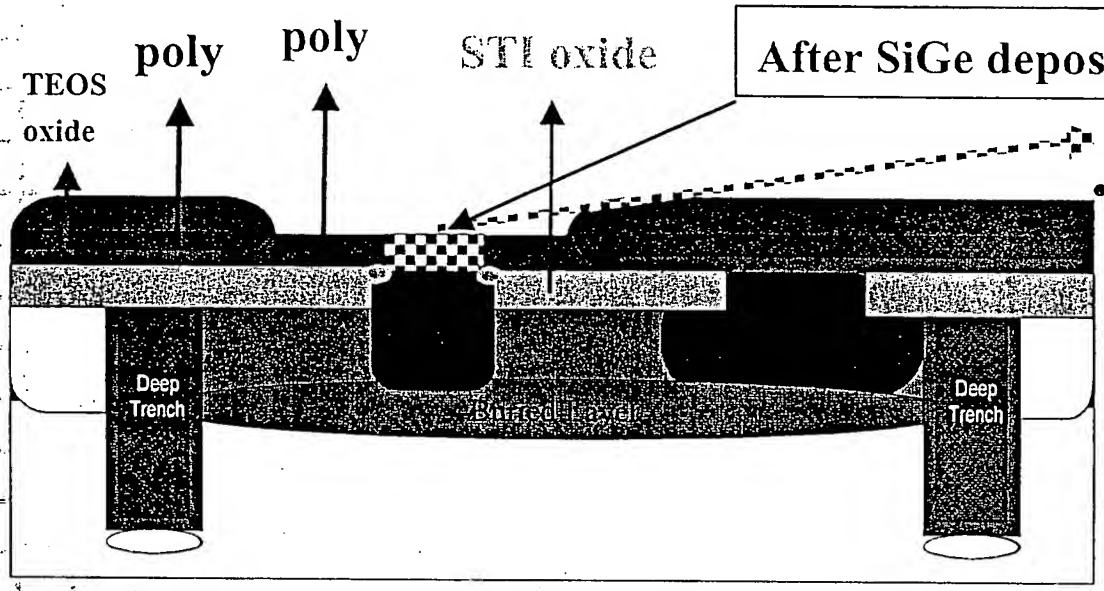
01-16P3

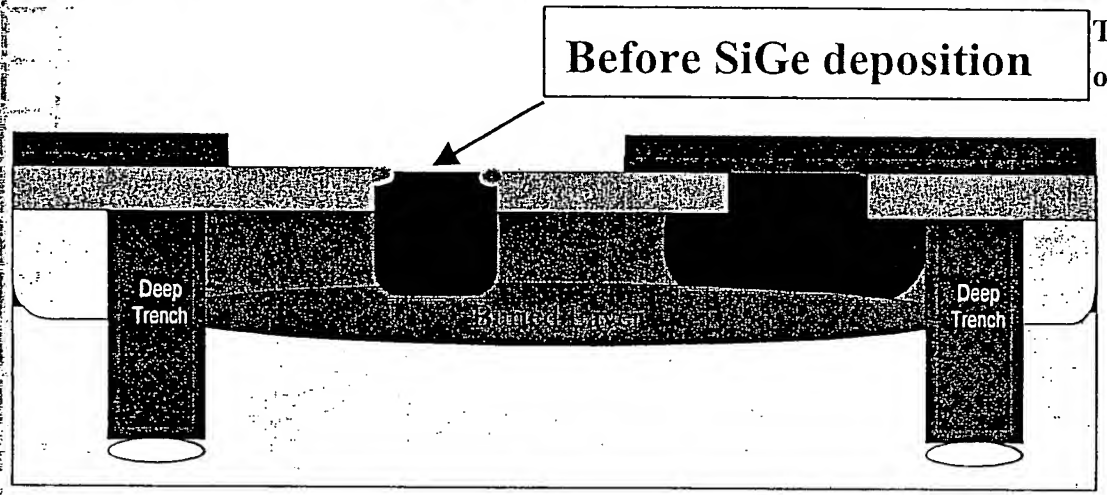
Introduction:

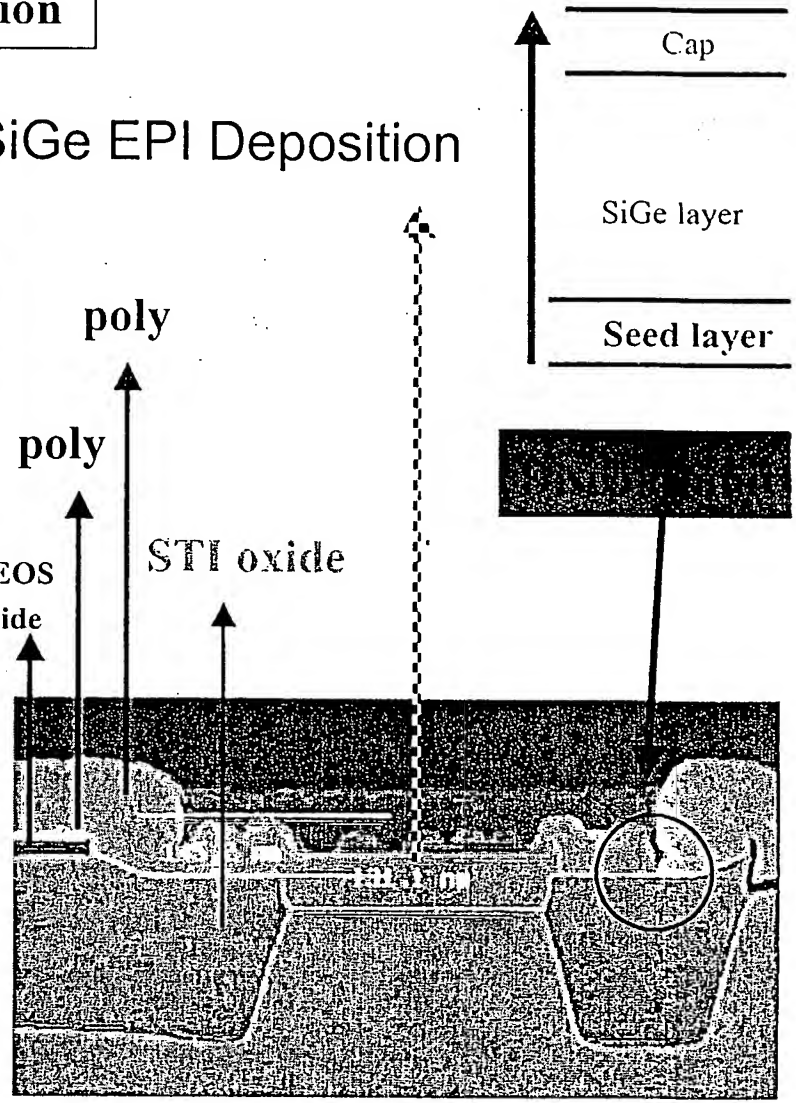
The discontinuity phenomenon present during SiGe deposition between Si/oxide/poly film will cause the poor poly sheet resistance connected with base electrode.

Figure 1 shows the discontinuity phenomenon with cross section view during SiGe deposition between Si/oxide/poly film.

Introduction:Discontinuity issue during SiGe deposition on Si/oxide/poly film







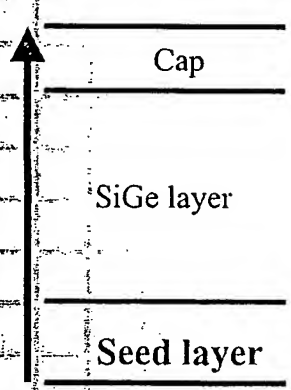
Method & Advantage:

This patent presents the methodology that only adjust the process temperature of seed layer, and keep the temperature of SiGe and cap deposition the same with standard recipe.The results were shown in Figure 3 and Figure 4 . That could gain two following advantages:

1. The discontinuity of seed layer was prevented just by process temperature adjustment and with throughput improvement.
2. The SiGe/B profile will not be changed due to the process temperature of SiGe and cap deposition keep the same.

Advantage: To prevent discontinuity during SiGe deposition on Si/oxide/poly film by temperature adjustment without changing SiGe/B profile.

Method: To adjust the process temperature of seed layer, and keep the temperature and duration of SiGe and cap deposition the same as standard recipe.



Deposition conditions optimization

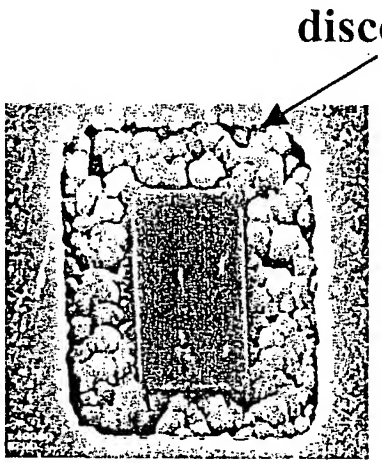


Fig. 1

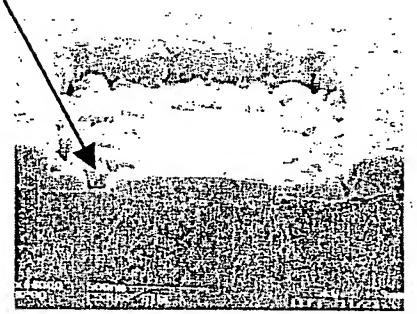


Fig. 2

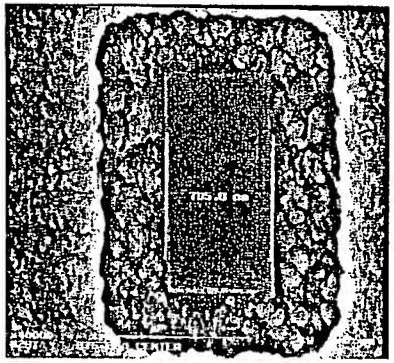


Fig. 3

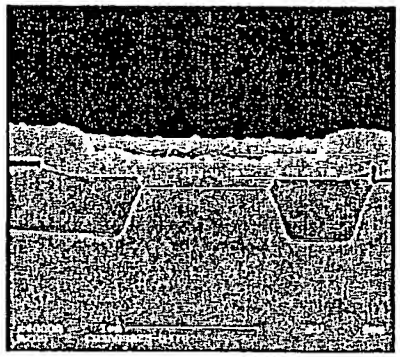


Fig. 4